

Application No. 09/749,405  
Amendment dated March \_\_, 2005  
Reply to Office Action of November 19, 2004

Atty. Docket No. 2207/7085  
Assignee: Intel Corporation

### **AMENDMENT TO THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application.

#### **What is claimed is:**

1. (Currently Amended) A branch prediction apparatus, comprising:  
a base misprediction history register ~~providing to provide~~ an output;  
a meta predictor to receive as inputs an index value and a branch prediction to generate a misprediction value in accordance with said inputs and said base misprediction history register output; and  
a logic gate to receive said branch prediction and said misprediction value to generate a final prediction.
2. (Original) The branch prediction apparatus of claim 1, wherein said base misprediction history register includes misprediction history data.
3. (Original) The branch prediction apparatus of claim 1, further comprising an instruction that provides said index value.
4. (Original) The branch prediction apparatus of claim 3, wherein said instruction is a branch instruction.
5. (Original) The branch prediction apparatus of claim 4, wherein said final prediction determines a branch for said branch instruction.
6. (Previously presented) The branch prediction apparatus of claim 1, further comprising a branch predictor that receives said index value and generates said branch prediction.

Application No. 09/749,405  
Amendment dated March \_\_, 2005  
Reply to Office Action of November 19, 2004

Atty. Docket No. 2207/7085  
Assignee: Intel Corporation

7. (Original) The branch prediction apparatus of claim 6, wherein said branch predictor utilizes a prediction scheme to generate said branch prediction.
8. (Original) The branch prediction apparatus of claim 6, wherein said branch predictor includes a target address field and a prediction table.
9. (Original) The branch prediction apparatus of claim 1, wherein said base misprediction history register contains values of zero (0), and the misprediction value is not generated by said meta predictor.
10. (Original) A method for predicting branches, comprising:  
receiving an index value, a branch prediction value correlating to said index value, and a misprediction history value at a meta predictor; and  
generating a misprediction value at said meta predictor.
11. (Original) The method of claim 10, further comprising generating said branch prediction value at a branch predictor.
12. (Original) The method of claim 11, further comprising receiving an index value at said branch predictor.
13. (Original) The method of claim 10, further comprising generating a final prediction according to said branch prediction and said misprediction value.
14. (Original) The method of claim 10, further comprising determining a final value, and updating said meta predictor and said base misprediction history register according to said final value.
15. (Original) The method of claim 14, wherein said updating includes comparing said final value to said branch prediction.

Application No. 09/749,405  
Amendment dated March \_\_, 2005  
Reply to Office Action of November 19, 2004

Atty. Docket No. 2207/7085  
Assignee: Intel Corporation

16. (Original) The method of claim 10, further comprising bypassing said meta predictor when said misprediction history value contains all zeros (0).
17. (Currently Amended) A processor, comprising:  
a branch predictor to generate a branch prediction;  
a base misprediction history register;  
a meta predictor ~~that receives~~ to receive an index value, said branch prediction and base misprediction history register data to generate a misprediction value.
18. (Original) The processor of claim 17, further comprising a final prediction to correlate to said misprediction value and said branch prediction value.
19. (Original) The processor of claim 17, further comprising a logic gate to generate said final prediction.
20. (Original) A computer readable medium having stored a plurality of executable instructions, the plurality of instructions comprising instructions to:  
receive an index value, a branch prediction value correlating to said index value, and a misprediction history value at a meta predictor; and  
generate a misprediction value at said meta predictor.
21. (Original) The computer readable medium of claim 20, further comprising an instruction to generate said branch prediction value at a branch predictor.
22. (Original) The computer readable medium of claim 21, further comprising an instruction to receive an index value at said branch predictor.
23. (Original) The computer readable medium of claim 19, further comprising an instruction to generate a final prediction according to said branch prediction and said misprediction value.

Application No. 09/749,405  
Amendment dated March \_\_, 2005  
Reply to Office Action of November 19, 2004

Atty. Docket No. 2207/7085  
Assignee: Intel Corporation

24. (Original) A method for restoring a branch prediction apparatus following a branch misprediction of a branch instruction, comprising:  
restoring a base misprediction history register; and  
restoring a branch predictor history register.
25. (Previously presented) The method of claim 24, further comprising updating a branch predictor.
26. (Original) The method of claim 24, further comprising updating a meta predictor.
27. (Original) The method of claim 24, further comprising flushing an instruction pipeline processing said branch instruction.